REMARKS

This amendment is responsive to the Office Action dated April 20, 2001. Attached hereto, therefore, are a request for a three-month extension of time and the appropriate fee.

Claims 1-24 and 28-32 are now pending. The Office Action rejects certain claims under 35 U.S.C. 112, second paragraph, rejects Claims 1, 2, 7-9, 13, 20, 21 and 23 under 35 U.S.C. 102(**e**)[1] as anticipated by U.S. Patent No. 6,083,811 to Riding, and rejects various other claim groups under 35 U.S.C. 103(a) as obvious over Riding in combination with one or more additional references.

Section 112 Rejections

Applicants have carefully amended certain ones of the claims to address each of the Examiner's Section 112 concerns:

Applicants have amended the preamble of Claim 1 to recite "a plurality of dies" to provide antecedent support for the reference to "said" plurality of dies at line 7 of amended claim 1.

---

[1] The Office Action indicates that the rejections is based on 35 USC 102(b), but during a telephone conference with Applicants' attorney, the Examiner kindly confirmed that the applicable section is 102(e), not 102(b).

Applicants have amended Claims 13, 23 and 24 to provide literal antecent basis for "said dies". In particular, Claim 13 now introduces "a die" that is "from said plurality of dies" and Claims 23 and 24 reference "said plurality of dies".

Applicants have resolved the antecedent problem with the reference to "said die" in Claims 14-16 by amending parent Claim 13 to introduce "a die" as noted above.

Applicants have resolved the antecedent problem with "said integrated circuit" in Claim 15 by amending the claim to recite "an integrated circuit".

Applicants have resolved the antecedent problem with Claim 16 by amending Claim 15 as just noted.

Applicants have resolved the antecedent problem with Claim 16's use of the phrase "a plurality of separated dies prepared by said method" to read "a plurality of dies manufactured by said method".

Finally, with regard to the use of the terms "low" in Claims 2, 3, 10, 18 and 19, Applicants have simply deleted those limitations from the claims. Claim 2, for example, now recites "a planarizing layer of material" rather than "a planarizing layer of *low stress* material".

The Examiner is invited to telephone the undersigned attorney if any further Section 112 concerns become apparent.

Rejections Based on Riding

As noted in the introductory portion of these remarks, all of the Office Action's rejections rely upon Riding as prior art. The Riding reference corresponds to U.S. Patent No. 6,083,811. It issued on July 4, 2000, long after the November 11, 1997 filing date of the provisional patent application no. 60/065,088 to which Applicants' claim benefit. Accordingly, the Riding patent is available as a prior art reference under 35 U.S.C. 102(e) based on its filing date. The "effective date" of the Riding patent, in other words, is February 7, 1996.

In accordance with the applicable statutes and rules therefore, Applicants have elected to swear behind Riding by submitting declarations that provide substantial evidence that their herein claimed invention was invented prior to the effective date of the Riding patent. That reference no longer being applicable as a prior art reference, it appears that the present case is substantively in condition for allowance.

Conclusion

It now appearing that this case is fully in condition for allowance, Applicants earnestly solicit a notice to that effect. Applicants invite the Examiner to call the undersigned attorney if it appears that a phone conference would further this case in any way.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on
October 22, 2001
Angela Williams

Signature
October 22, 2001

Respectfully submitted,

Joseph C. Andras
Registration No. 33,469
Myers, Dawes & Andras LLP
19900 MacArthur Blvd, Suite 1150
Irvine, CA 92612

Appendix of Amended Claims With Amendments Shown

1. (Twice Amended) A method for manufacturing a plurality of **dies containing** thinned integrated circuits from a semiconductor wafer having a thickness, a front surface and a backside surface, comprising:

defining a plurality of grooves into said front surface of said semiconductor wafer to define said plurality of dies, said grooves penetrating into said surface at a predetermined distance less than said thickness of said semiconductor wafer so that said plurality of dies remain integral with said wafer;

mounting said wafer to a flat rigid substrate to support said wafer, said wafer being mounted to said substrate with said front surface turned toward said substrate;

mechanically removing a predetermined portion of said backside of said wafer until said thickness of said wafer is reduced to expose said plurality of grooves to said backside in preparation to separating said plurality of said dies, said dies remaining mounted to said substrate; and

releasing said plurality of dies from said substrate.

2. (Amended) The method of claim 1 further comprising disposing a planarizing layer of ~~low stress~~ material on said front surface of said wafer into which said plurality of grooves have been defined prior to mounting said front surface of said wafer to said flat substrate.

3. (Amended) The method of claim 1 further comprising disposing a layer of ~~low stress~~ material on said front surface of said wafer before defining said plurality of grooves into said front surface of said wafer.

10. (Amended) The method of claim 1 wherein mounting said wafer to said flat substrate comprises affixing said wafer by means of ~~a low viscosity low stress~~ an adhesive.

13. (Amended) The method of claim 1 further comprising mounting a die from said plurality of dies onto a flexible film.

15. (Amended) The method of claim 13 where mounting said die on said flexible film further comprises electrically coupling ~~said~~ an integrated circuit in said die to metalizations provided on said film.

18. (Amended) The method of claim 17 wherein affixing said front surface to said flat substrate comprises affixing said front surface using ~~low viscosity, low stress materials~~ an adhesive material disposed between said front surface and said flat substrate.

19. (Amended) The method of claim 18 further comprising pressing said wafer and substrate together with said ~~low viscosity and low stress~~ **adhesive** material therebetween and curing said **adhesive** material while maintaining said pressure between said wafer and substrate.

23. (Amended) The method of claim 1 where defining said plurality of grooves in said front surface of said wafer comprises defining linear grooves into said front surface of said wafer in an intersecting grid pattern to define each of said **plurality of** dies, thereby isolating each die by a surrounding moat of stress relieving grooves.

24. (Amended) The method of claim 1 further comprising stacking a plurality of ~~separated~~ dies ~~prepared~~ **manufactured** by said method, and electrically interconnecting said **plurality of** dies.

~~25. (Cancel) An assembly used for manufacturing a plurality of thinned integrated circuits from a semiconductor wafer having a thickness, a front surface and a backside surface, comprising:~~

~~a plurality of grooves defined into said front surface of said semiconductor wafer to define said plurality of dies, said grooves penetrating into said front surface a predetermined distance which is less than said~~

~~thickness of said semiconductor wafer so that said plurality of dies remain integral with said wafer; and~~

~~a flat rigid substrate mounted to said wafer to support said wafer, said wafer being mounted to said substrate with said front surface turned toward said substrate and to expose said backside of said wafer for partial mechanical removal of said backside by an amount sufficient to expose said plurality of grooves to said backside in preparation to separating said plurality of said dies, said dies remaining of mounted to said substrate.~~

~~26. (Cancel) The assembly of claim 25 further comprising a low viscosity, low stress layer disposed between said front surface of said wafer and said substrate to affix said front surface of said wafer to said substrate.~~

~~27. (Cancel) The assembly of claim 26 wherein said low viscosity, low stress layer includes a polyimide layer disposed on said front surface.~~